AMITABH YADAV

Electronics & Computer Engineer

Nationality: Indian · D.O.B. March 27, 1995

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EDUCATION

Delft University of Technology, Netherlands *September 2017 - August 2019*
Master of Science (M.Sc.) in Computer Engineering/EEMCS Overall GPA: 8.2/10.0

- Thesis: 'Micro-architecture Design for Spin-Qubit Quantum Processor'. Grade: 9/10 (1 year)
- Design and Jitter Analysis of Quadrature Phase By-6 frequency divider in Cadence Spectre.
- Performance improvement of Plasma processor core (opencores.org) in VHDL.
- BICMOS5 Fabrication & Measurement of IC parameters in EKL Cleanroom, TU Delft.
- Running Shor's Algorithm on IBM Quantum Experience using IBM-Q QISKit.
- Parallel Poisson Solver on Distributed Memory HPC cluster using MPI.
- Development of Classic Snake Game using Software Design Patterns in Java.

University of Petroleum and Energy Studies, India *August 2013 - June 2017*
Bachelor of Technology (B.Tech.) in Electronics Engineering/EE Dept. Overall GPA: 3.1/4.0

- 'Design and Simulation of 16-bit Microcontroller in VHDL/Xilinx ISE'. Grade: 4/4 (8 Months)
- 'Embedded Hardware for Audio Morse-Code Encoder/Decoder'. Grade: 4/4 (4 months)
- Others: Head of University Discipline Committee to successfully ensure Anti-Ragging, Gender Sensitization, Anti Substance Abuse, and Road Traffic Safety,
  Class Representative of Electronics Engineering (class of 2017) for all 4 years of UG studies,
  IT & Design Head of UPES-IEEE Student Chapter.

EXPERIENCE

LBNL (Lawrence Berkeley National Laboratory) November 2019 - present
Research Associate - HEP.QPR *Berkeley, California*

- Quantum Algorithms development for HEP Charged-Particle Track Reconstruction.
- Audit Course: "EE290-2 Hardware for Machine Learning" at UC Berkeley (ongoing).
- Activities: Simons Institute for the Theory of Computing, Advanced Quantum Testbed (AQT), LBNL.

QuTech/Intel Quantum Computing Lab September 2018 - August 2019
Master Thesis Research (under N. Khammassi (Intel, Oregon), K. Bertels (QuTech)) Delft, Netherlands

- Complete **CC-Spin Micro-architecture** development in Verilog and C.
- Central Controller (CC-Spin) hardware implemented on Cyclone-V SoC-FPGA is dedicated for translating the Instruction Set (QISA) to sequences of arbitrary I/Q and DC Pulses. CC-Spin is connected in Star-topology with FPGA-controlled Direct Digital Synthesis (DDS) units via LVDS links for multi-channel synchronous waveform generation.
- Design of Quantum Instruction Pipeline, Microcode Unit, 8b/10b Encoder/Decoder, SERDES, Timing Control Unit and SPI Master (DDS controller) to perform Qubit rotations with precise timing.

DARE (Delft Aerospace Rocket Engineering) - Stratos-III October 2017 - July 2018
Electronics/Firmware Engineer - Core Team Member *Delft, Netherlands*

- Avionics Hardware development on ARM Cortex-M3/LPC1768 MCU and PCB Design of using Altium Designer 18 for Stratos-III Sounding Rocket.

CERN (European Organization for Nuclear Research) June 2017 - August 2017
Summer Student - ATLAS Pixel Group/EP-ADE-ID (under C. Solans, A. Sharma) Geneva, Switzerland

- Development of front-end DAQ firmware for FEI-4 Silicon Pixel Chip for ATLAS ITk on Xilinx KC705.
- Integrated IPBus (UDP/IP) (front-end monitoring) with 8b/10b encoded Rx/Tx Core to communicate with back-end Gigabit TRx (GBT) protocol. Developed the data_routing entity 'E_Link Bank'.

BARC (Bhabha Atomic Research Center) June 2016 - July 2016
Project Trainee - Data Acquisition & Processing Systems Group (under A. Dohare) *Mumbai, India*

- Developed Lossless Compression library for A, B and C Scan Ultrasonic Scan Data for application in NDT of Materials (achieved 75.37% compression in C-Scan).

TECHNICAL STRENGTHS

Programming	C, Java, Python (NumPy, MatPlotLib), CUDA, MATLAB Verilog and VHDL
Software & Tools	Quartus Prime, Vivado/ISE, LTSPICE, Altium Designer, LaTeX, Cadence Spectre, QISKit
MOOCs/Summer Schools	Particle Physics: Introduction, Quantum Cryptography, Quantum Machine Learning, Quantum Computing for High Energy Physics (CERN), Quantum Information for Developers 2018 (ETH Zurich)

PUBLICATIONS

1. *"A Micro-architecture design for scalable control of Spin-Qubit Quantum Processor"* (2020)
2. *"Quantum Computer Architecture: Towards Full-Stack Quantum Accelerators"* (2019)
3. *"FE-I4 Firmware Development and Integration with FELIX for the Pixel Detector"* (2017)
4. *"Wireless Sensor Network Based Patient Health Monitoring and Tracking System"* (2017)

NATIONAL AND INTERNATIONAL ACHIEVEMENTS

- National Rank #1 (jointly with IIT Madras), Critical Design Phase (Phase-II) of C130-J Super Hercules Aircraft Roll-On/Roll-Off Design Challenge. A grant of USD 65,000 was awarded by Lockheed Martin for design prototyping in colaboration with TASL, IAF and NDRF.
- Rank 1st as Team's Technical Advisor at International CANSAT Competition 2017 at Texas, USA. Rank 4th (Rank #1 in Europe, Asia) as Team Leader (Electronics) at CANSAT 2016.
- Competed at the world's largest student-built rocketry competiton IREC, as Chief Electronics and Payload Engineer of 'Kalam' Sounding Rocket, developed by Team Garud, Rocketry Division of UPES.
- Ranked #1st and #8th at University Best Research Awards in 2017 and 2016, respectively. Wireless Sensor Network (WSN) system for Landslide Forecasting in the Himalayan Regions (2017), WSN Heath Monitoring and Indoor Location Tracking (2016) (Funded by UPES-RISE).